

# DATA SHEET



## **PCA9554/PCA9554A**

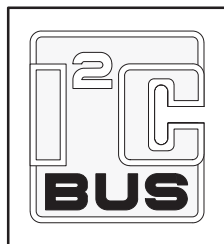
8-bit I<sup>2</sup>C and SMBus I/O port with interrupt

Product data  
Supersedes data of 2002 May 13

2002 Jul 26

8-bit I<sup>2</sup>C and SMBus I/O port with interrupt

## PCA9554/PCA9554A



## FEATURES

- Operating power supply voltage range of 2.3 to 5.5 V
- 5 V tolerant I/Os
- Polarity inversion register
- Active low interrupt output
- Low stand-by current
- Noise filter on SCL/SDA inputs
- No glitch on power-up
- Internal power-on reset
- 8 I/O pins which default to 8 inputs
- 0 to 400 kHz clock frequency
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JESDEC Standard JESD78 which exceeds 100 mA
- Four packages offered: SO16, SSOP16, TSSOP16, and HVQFN16

## DESCRIPTION

The PCA9554 and PCA9554A are 16-pin CMOS devices that provide 8 bits of General Purpose parallel Input/Output (GPIO) expansion for I<sup>2</sup>C/SMBus applications and were developed to enhance the Philips family of I<sup>2</sup>C I/O expanders. The improvements include higher drive capability, 5V I/O tolerance, lower supply current, individual I/O configuration, 400 kHz clock frequency, and smaller packaging. I/O expanders provide a simple solution when additional I/O is needed for ACPI power switches, sensors, pushbuttons, LEDs, fans, etc..

The PCA9554/54A consist of an 8-bit Configuration register (Input or Output selection); 8-bit Input register, 8-bit Output register and an 8-bit Polarity inversion register (Active high or Active low operation). The system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each Input or Output is kept in the corresponding Input or Output register. The polarity of the read register can be inverted with the Polarity Inversion Register. All registers can be read by the system master. Although pin to pin and I<sup>2</sup>C address compatible with the PCF8574 series, software changes are required due to the enhancements and are discussed in Application Note AN469.

The PCA9554/54A open-drain interrupt output is activated when any input state differs from its corresponding input port register state and is used to indicate to the system master that an input state has changed. The power-on reset sets the registers to their default values and initializes the device state machine.

Three hardware pins (A0, A1, A2) vary the fixed I<sup>2</sup>C address and allow up to eight devices to share the same I<sup>2</sup>C/SMBus. The PCA9554A is identical to the PCA9554 except that the fixed I<sup>2</sup>C address is different allowing up to sixteen of these devices (eight of each) on the same I<sup>2</sup>C/SMBus.

## ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	TOPSIDE MARK	DRAWING NUMBER
16-Pin Plastic SO (wide)	-40 to +85 °C	PCA9554D	PCA9554D	SOT162-1
16-Pin Plastic SSOP	-40 to +85 °C	PCA9554DB	9554DB	SOT338-1
16-Pin Plastic TSSOP	-40 to +85 °C	PCA9554PW	9554DH	SOT403-1
16-Pin Plastic HVQFN	-40 to +85 °C	PCA9554BS	9554	SOT629-1
16-Pin Plastic SO (wide)	-40 to +85 °C	PCA9554AD	PCA9554AD	SOT162-1
16-Pin Plastic SSOP	-40 to +85 °C	PCA9554ADB	9554A	SOT338-1
16-Pin Plastic TSSOP	-40 to +85 °C	PCA9554APW	9554ADH	SOT403-1
16-Pin Plastic HVQFN	-40 to +85 °C	PCA9554ABS	554A	SOT629-1

Standard packing quantities and other packaging data are available at [www.philipslogic.com/packaging](http://www.philipslogic.com/packaging).

I<sup>2</sup>C is a trademark of Philips Semiconductors Corporation.

SMBus as specified by the Smart Battery System Implementers Forum is a derivative of the Philips I<sup>2</sup>C patent.

# 8-bit I<sup>2</sup>C and SMBus I/O port with interrupt

# PCA9554/PCA9554A

## PIN CONFIGURATION — SO, SSOP, TSSOP

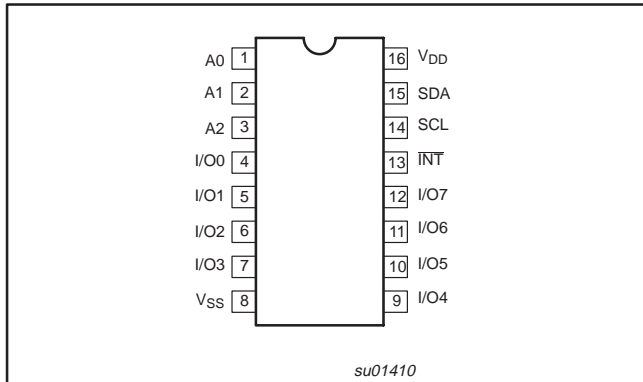


Figure 1. Pin configuration — SO, SSOP, TSSOP

## PIN CONFIGURATION — HVQFN

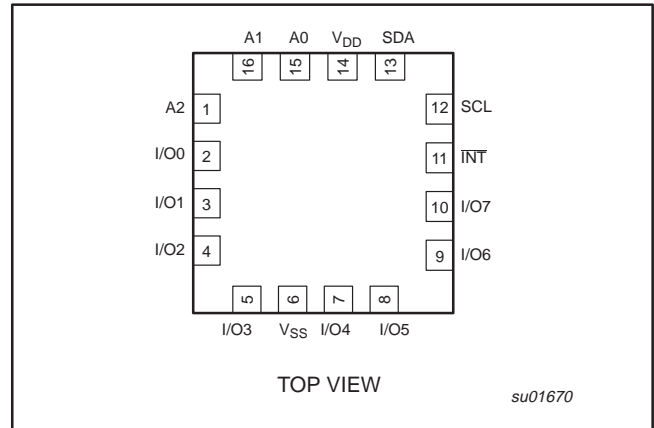


Figure 2. Pin Configuration — HVQFN

## PIN DESCRIPTION

SO, SSOP, TSSOP PIN NUMBER	HVQFN PIN NUMBER	SYMBOL	FUNCTION
1	15	A0	Address input 0
2	16	A1	Address input 1
3	1	A2	Address input 2
4–7	2–5	I/O0–3	I/O0 to I/O3
8	6	V <sub>SS</sub>	Supply ground
9	7–10	I/O4–7	I/O4 to I/O7
13	11	INT	Interrupt output (open drain)
14	12	SCL	Serial clock line
15	13	SDA	Serial data line
16	14	V <sub>DD</sub>	Supply voltage

## BLOCK DIAGRAM

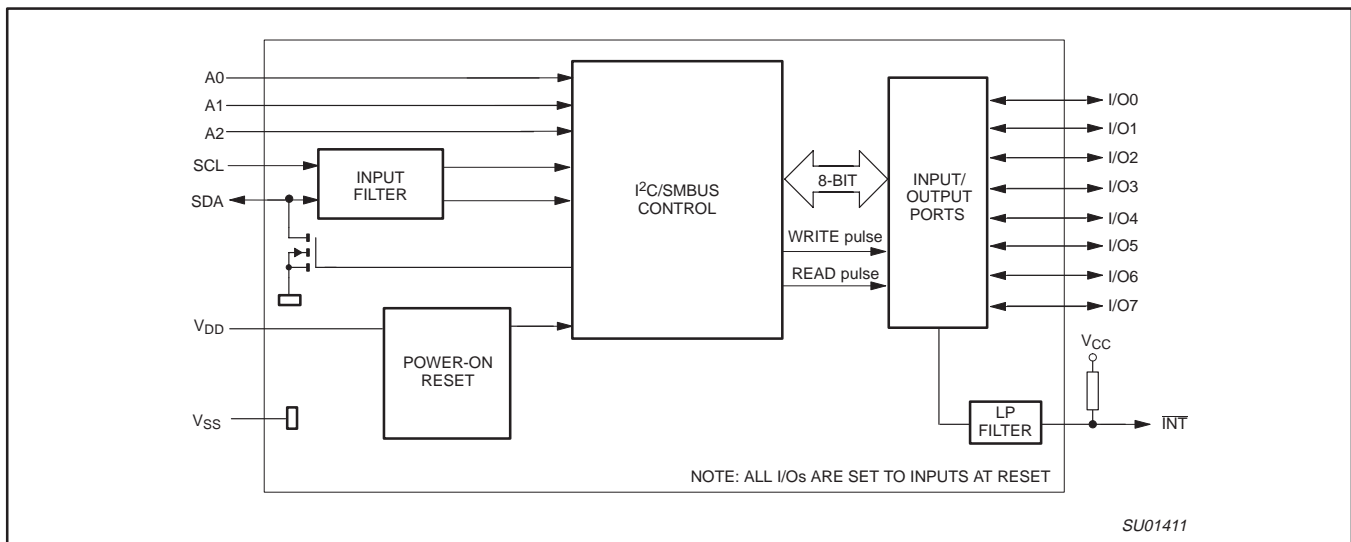


Figure 3. Block diagram

8-bit I<sup>2</sup>C and SMBus I/O port with interrupt

## PCA9554/PCA9554A

**REGISTERS****Command Byte**

Command	Protocol	Function
0	Read byte	Input port register
1	Read/write byte	Output port register
2	Read/write byte	Polarity inversion register
3	Read/write byte	Configuration register

The command byte is the first byte to follow the address byte during a write transmission. It is used as a pointer to determine which of the following registers will be written or read.

**Register 0 – Input Port Register**

bit	I7	I6	I5	I4	I3	I2	I1	I0
default	1	1	1	1	1	1	1	1

This register is a read only port. It reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by Register 3. Writes to this register have no effect.

**Register 1 – Output Port Register**

bit	O7	O6	O5	O4	O3	O2	O1	O0
default	1	1	1	1	1	1	1	1

This register reflects the outgoing logic levels of the pins defined as outputs by Register 3. Bit values in this register have no effect on pins defined as inputs. Reads from this register return the value that is in the flip-flop controlling the output selection, NOT the actual pin value.

**Register 2 – Polarity Inversion Register**

bit	N7	N6	N5	N4	N3	N2	N1	N0
default	0	0	0	0	0	0	0	0

This register allows the user to invert the polarity of the Input Port Register data. If a bit in this register is set (written with '1'), the corresponding Input Port data is inverted. If a bit in this register is cleared (written with a '0'), the Input Port data polarity is retained.

**Register 3 – Configuration Register**

bit	C7	C6	C5	C4	C3	C2	C1	C0
default	1	1	1	1	1	1	1	1

This register configures the directions of the I/O pins. If a bit in this register is set, the corresponding port pin is enabled as an input with high impedance output driver. If a bit in this register is cleared, the corresponding port pin is enabled as an output. At reset, the I/Os are configured as inputs with a weak pull-up to V<sub>DD</sub>.

**Power-on Reset**

When power is applied to V<sub>DD</sub>, an internal power-on reset holds the PCA9554 in a reset state until V<sub>DD</sub> has reached V<sub>POR</sub>. At that point, the reset condition is released and the PCA9554 registers and state machine will initialize to their default states.

**Interrupt Output**

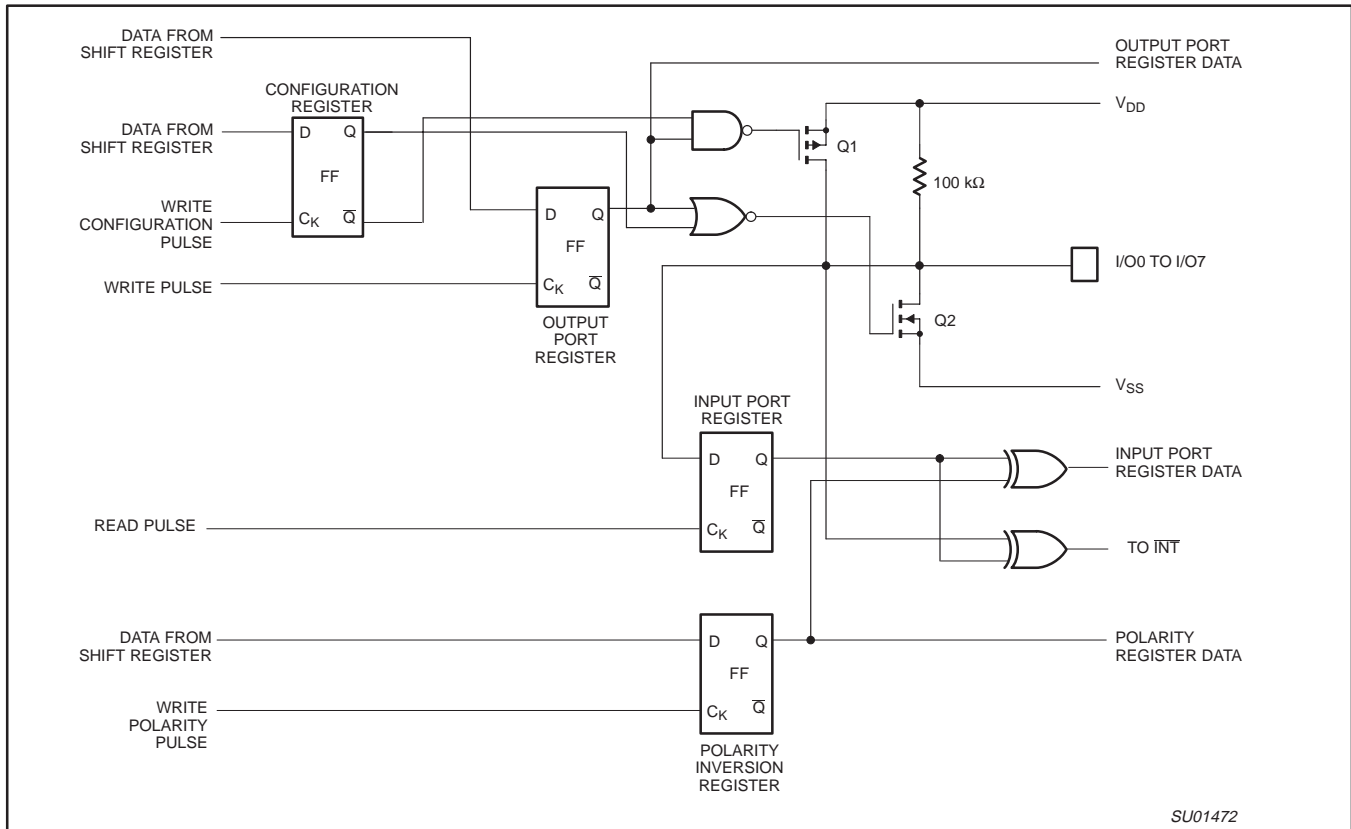
The open-drain interrupt output is activated when one of the port pins change state and the pin is configured as an input. The interrupt is deactivated when the input returns to its previous state or the input port register is read.

Note that changing an I/O from an output to an input may cause a false interrupt to occur if the state of the pin does not match the contents of the input port register.

# 8-bit I<sup>2</sup>C and SMBus I/O port with interrupt

# PCA9554/PCA9554A

## SIMPLIFIED SCHEMATIC OF I/O0 TO I/O7



SU01472

**NOTE:** At Power-on Reset, all registers return to default values.

**Figure 4. Simplified schematic of I/O0 to I/O7**

### I/O port

When an I/O is configured as an input, FETs Q1 and Q2 are off, creating a high impedance input with a weak pull-up (100 kΩ typ.) to V<sub>DD</sub>. The input voltage may be raised above V<sub>DD</sub> to a maximum of 5.5 V.

If the I/O is configured as an output, then either Q1 or Q2 is enabled, depending on the state of the output port register. Care should be exercised if an external voltage is applied to an I/O configured as an output because of the low impedance paths that exist between the pin and either V<sub>DD</sub> or V<sub>SS</sub>.

# 8-bit I<sup>2</sup>C and SMBus I/O port with interrupt

# PCA9554/PCA9554A

## Device address

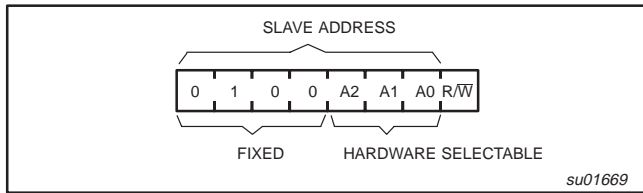


Figure 5. PCA9554 address

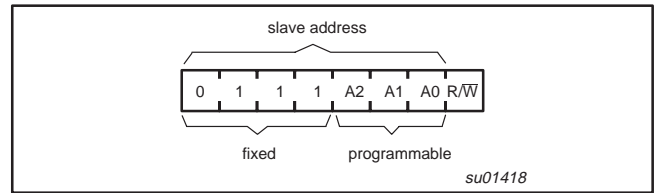


Figure 6. PCA9554A address

## Bus transactions

Data is transmitted to the PCA9554/PCA9554A registers using the write mode as shown in Figures 7 and 8. Data is read from the PCA9554/PCA9554A registers using the read mode as shown in Figures 9 and 10. These devices do not implement an auto-increment function so once a command byte has been sent, the register which was addressed will continue to be accessed by reads until a new command byte has been sent.

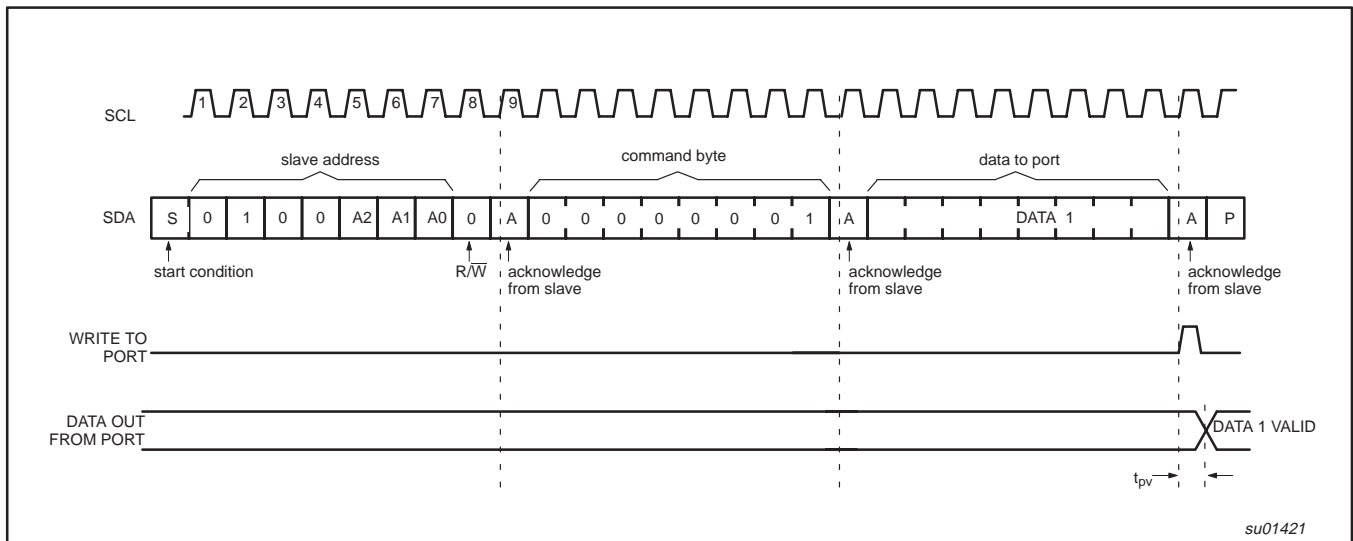


Figure 7. WRITE to output port register

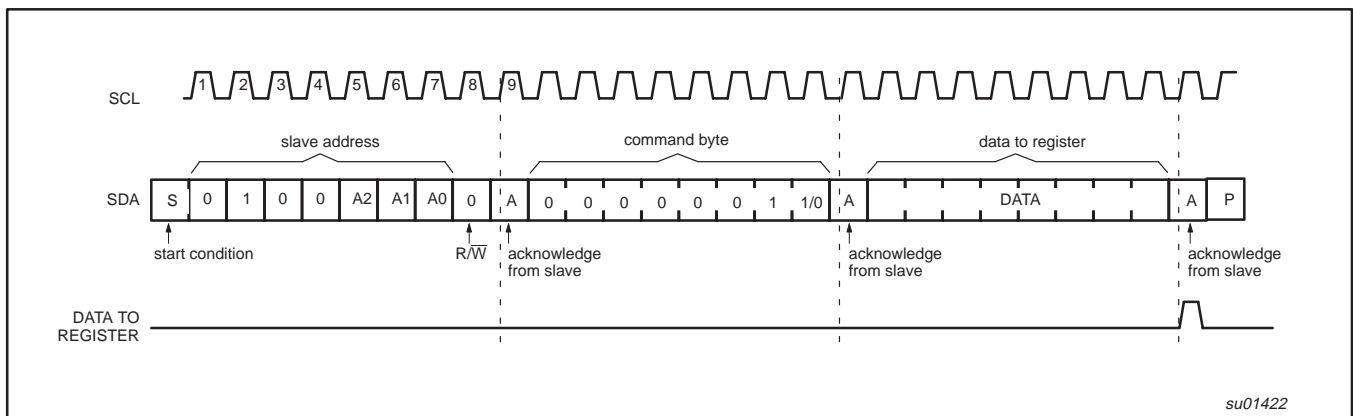


Figure 8. WRITE to configuration or polarity inversion registers

# 8-bit I<sup>2</sup>C and SMBus I/O port with interrupt

# PCA9554/PCA9554A

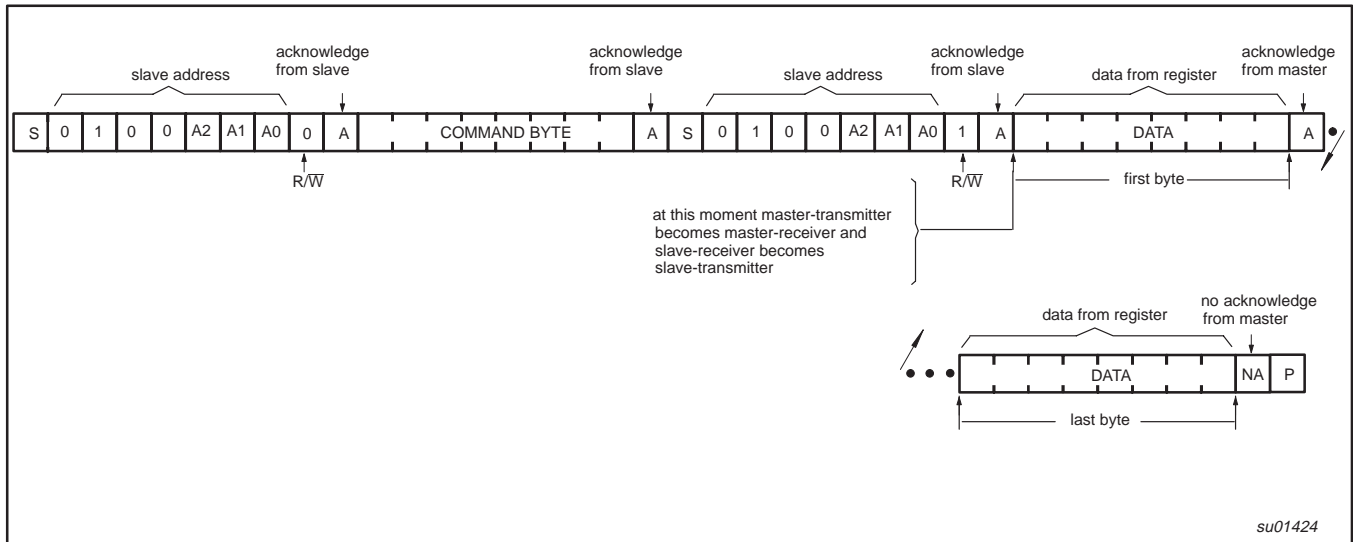
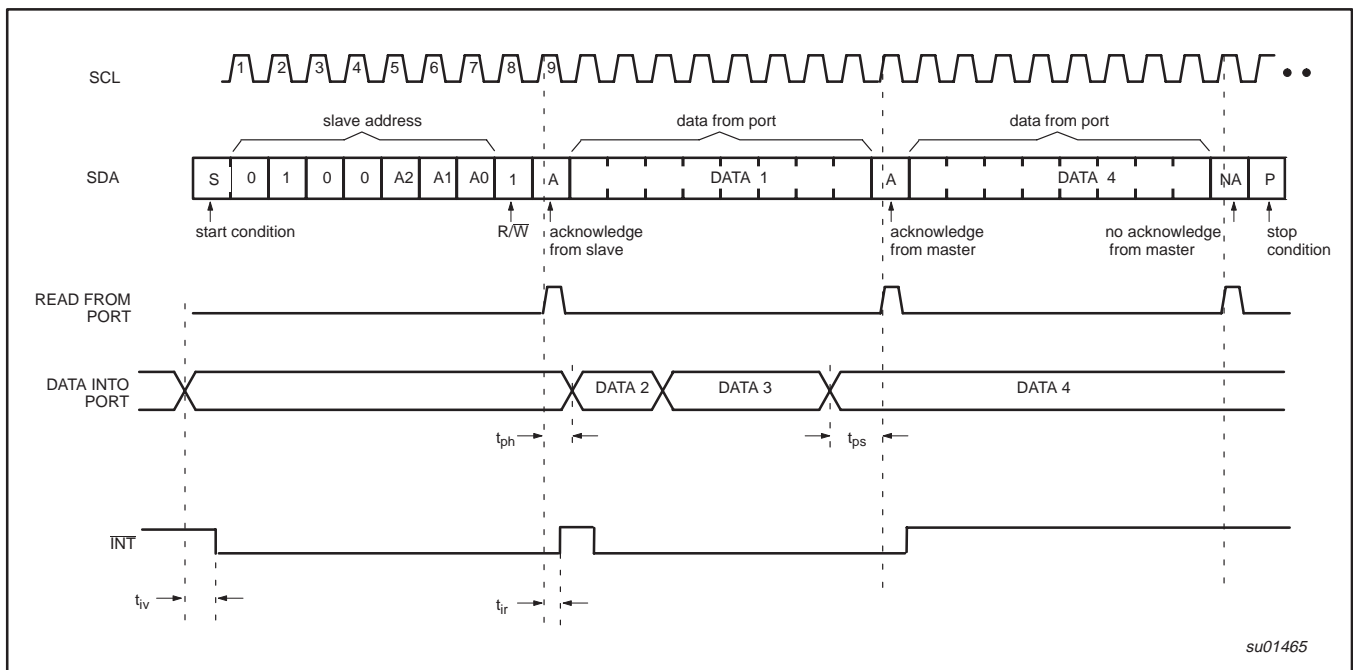


Figure 9. READ from register



**NOTES:**

1. This figure assumes the command byte has previously been programmed with 00h.
2. Transfer of data can be stopped at any moment by a stop condition.

Figure 10. READ input port register

8-bit I<sup>2</sup>C and SMBus I/O port with interrupt

## PCA9554/PCA9554A

**ABSOLUTE MAXIMUM RATINGS**

In accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V <sub>DD</sub>	Supply voltage		-0.5	6.0	V
I <sub>I</sub>	DC input current		—	±20	mA
V <sub>I/O</sub>	DC voltage on an I/O		V <sub>SS</sub> - 0.5	5.5	V
I <sub>I/O</sub>	DC output current on an I/O		—	±50	mA
I <sub>DD</sub>	Supply current		—	85	mA
I <sub>SS</sub>	Supply current		—	100	mA
P <sub>tot</sub>	Total power dissipation		—	200	mW
T <sub>stg</sub>	Storage temperature range		-65	+150	°C
T <sub>amb</sub>	Operating ambient temperature		-40	+85	°C



8-bit I<sup>2</sup>C and SMBus I/O port with interrupt

## PCA9554/PCA9554A

**HANDLING**

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take precautions appropriate to handling MOS devices. Advice can be found in Data Handbook IC24 under "Handling MOS devices".

**DC CHARACTERISTICS**

$V_{DD} = 2.3$  to  $5.5$  V;  $V_{SS} = 0$  V;  $T_{amb} = -40$  to  $+85$  °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
<b>Supplies</b>						
$V_{DD}$	Supply voltage		2.3	—	5.5	V
$I_{DD}$	Supply current	Operating mode; $V_{DD} = 5.5$ V; no load; $f_{SCL} = 100$ kHz	—	104	175	$\mu$ A
$I_{stbl}$	Standby current	Standby mode; $V_{DD} = 5.5$ V; no load; $V_I = V_{SS}$ ; $f_{SCL} = 0$ kHz; I/O = inputs	—	550	700	$\mu$ A
$I_{stbh}$	Standby current	Standby mode; $V_{DD} = 5.5$ V; no load; $V_I = V_{DD}$ ; $f_{SCL} = 0$ kHz; I/O = inputs	—	0.25	1	$\mu$ A
$V_{POR}$	Power-on reset voltage	No load; $V_I = V_{DD}$ or $V_{SS}$	—	1.5	1.65	V
<b>input SCL; input/output SDA</b>						
$V_{IL}$	LOW level input voltage		-0.5	—	$0.3 V_{DD}$	V
$V_{IH}$	HIGH level input voltage		$0.7 V_{DD}$	—	5.5	V
$I_{OL}$	LOW level output current	$V_{OL} = 0.4$ V	3	—	—	mA
$I_L$	Leakage current	$V_I = V_{DD} = V_{SS}$	-1	—	+1	$\mu$ A
$C_I$	Input capacitance	$V_I = V_{SS}$	—	6	10	pF
<b>I/Os</b>						
$V_{IL}$	LOW level input voltage		-0.5	—	0.8	V
$V_{IH}$	HIGH level input voltage		2.0	—	5.5	V
$I_{OL}$	LOW level output current	$V_{OL} = 0.5$ V; $V_{DD} = 2.3$ V; Note 1	8	10	—	mA
		$V_{OL} = 0.7$ V; $V_{DD} = 2.3$ V; Note 1	10	13	—	mA
		$V_{OL} = 0.5$ V; $V_{DD} = 4.5$ V; Note 1	8	17	—	mA
		$V_{OL} = 0.7$ V; $V_{DD} = 4.5$ V; Note 1	10	24	—	mA
		$V_{OL} = 0.5$ V; $V_{DD} = 3.0$ V; Note 1	8	14	—	mA
		$V_{OL} = 0.7$ V; $V_{DD} = 3.0$ V; Note 1	10	19	—	mA
$V_{OH}$	HIGH level output voltage	$I_{OH} = -8$ mA; $V_{DD} = 2.3$ V; Note 2	1.8	—	—	V
		$I_{OH} = -10$ mA; $V_{DD} = 2.3$ V; Note 2	1.7	—	—	V
		$I_{OH} = -8$ mA; $V_{DD} = 3.0$ V; Note 2	2.6	—	—	V
		$I_{OH} = -10$ mA; $V_{DD} = 3.0$ V; Note 2	2.5	—	—	V
		$I_{OH} = -8$ mA; $V_{DD} = 4.75$ V; Note 2	4.1	—	—	V
		$I_{OH} = -10$ mA; $V_{DD} = 4.75$ V; Note 2	4.0	—	—	V
$I_{IH}$	Input leakage current	$V_{DD} = 3.6$ V; $V_I = V_{DD}$	—	—	1	$\mu$ A
$I_{IL}$	Input leakage current	$V_{DD} = 5.5$ V; $V_I = V_{SS}$	—	—	-100	$\mu$ A
$C_I$	Input capacitance		—	3.7	5	pF
$C_O$	Output capacitance		—	3.7	5	pF
<b>Interrupt INT</b>						
$I_{OL}$	LOW level output current	$V_{OL} = 0.4$ V	3	—	—	mA
<b>Select Inputs A0, A1, A2</b>						
$V_{IL}$	LOW level input voltage		-0.5	—	0.8	V
$V_{IH}$	HIGH level input voltage		2.0	—	5.5	V
$I_{LI}$	Input leakage current		-1	—	1	$\mu$ A

**NOTES:**

- The total current sunk by all I/Os must be limited to 100 mA.
- The total current sourced by all I/Os must be limited to 85 mA.

# 8-bit I<sup>2</sup>C and SMBus I/O port with interrupt

# PCA9554/PCA9554A

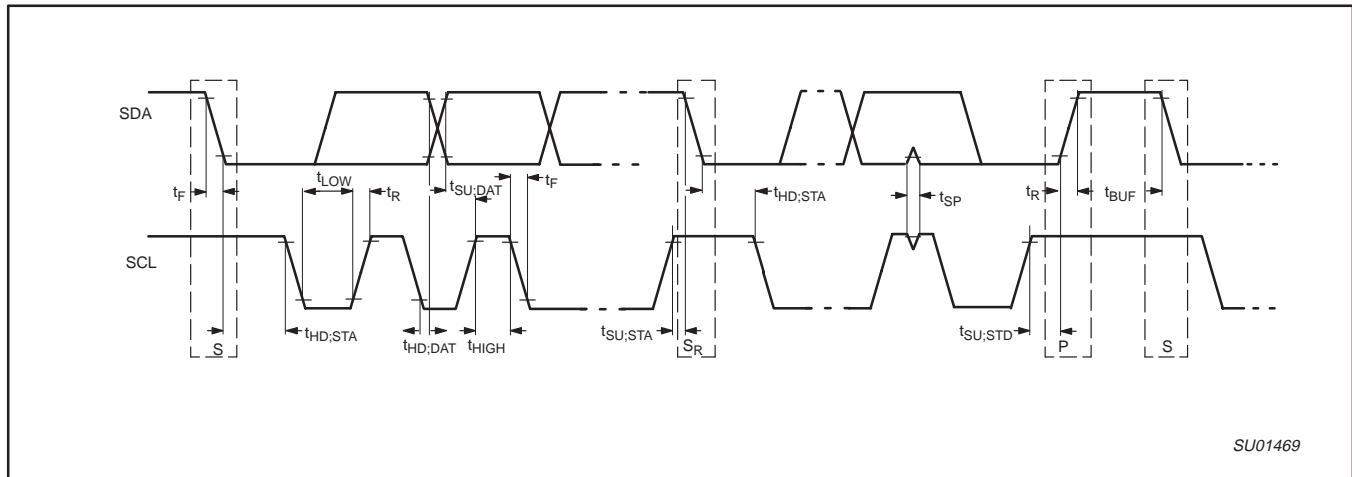


Figure 11. Definition of timing

## AC SPECIFICATIONS

SYMBOL	PARAMETER	STANDARD MODE I <sup>2</sup> C BUS		FAST MODE I <sup>2</sup> C BUS		UNITS
		MIN	MAX	MIN	MAX	
$f_{SCL}$	Operating frequency	0	100	0	400	kHz
$t_{BUF}$	Bus free time between STOP and START conditions	4.7	—	1.3	—	$\mu$ s
$t_{HD,STA}$	Hold time after (repeated) START condition	4.0	—	0.6	—	$\mu$ s
$t_{SU,STA}$	Repeated START condition setup time	4.7	—	0.6	—	$\mu$ s
$t_{SU,STO}$	Setup time for STOP condition	4.0	—	0.6	—	$\mu$ s
$t_{HD,DAT}$	Data in hold time	0	—	0	—	ns
$t_{VD,ACK}$	Valid time for ACK condition <sup>2</sup>	0.3	3.45	0.1	0.9	$\mu$ s
$t_{VD,DAT}$	Data out valid time <sup>3</sup>	300	—	50	—	ns
$t_{SU,DAT}$	Data setup time	250	—	100	—	ns
$t_{LOW}$	Clock LOW period	4.7	—	1.3	—	$\mu$ s
$t_{HIGH}$	Clock HIGH period	4.0	—	0.6	—	$\mu$ s
$t_F$	Clock/Data fall time	—	300	$20 + 0.1 C_b^1$	300	ns
$t_R$	Clock/Data rise time	—	1000	$20 + 0.1 C_b^1$	300	ns
$t_{SP}$	Pulse width of spikes that must be suppressed by the input filters	—	50	—	50	ns
<b>Port Timing</b>						
$t_{PV}$	Output data valid	—	200	—	200	ns
$t_{PS}$	Input data setup time	100	—	100	—	ns
$t_{PH}$	Input data hold time	1	—	1	—	$\mu$ s
<b>Interrupt Timing</b>						
$t_{IV}$	Interrupt valid	—	4	—	4	$\mu$ s
$t_{IR}$	Interrupt reset	—	4	—	4	$\mu$ s

**NOTES:**

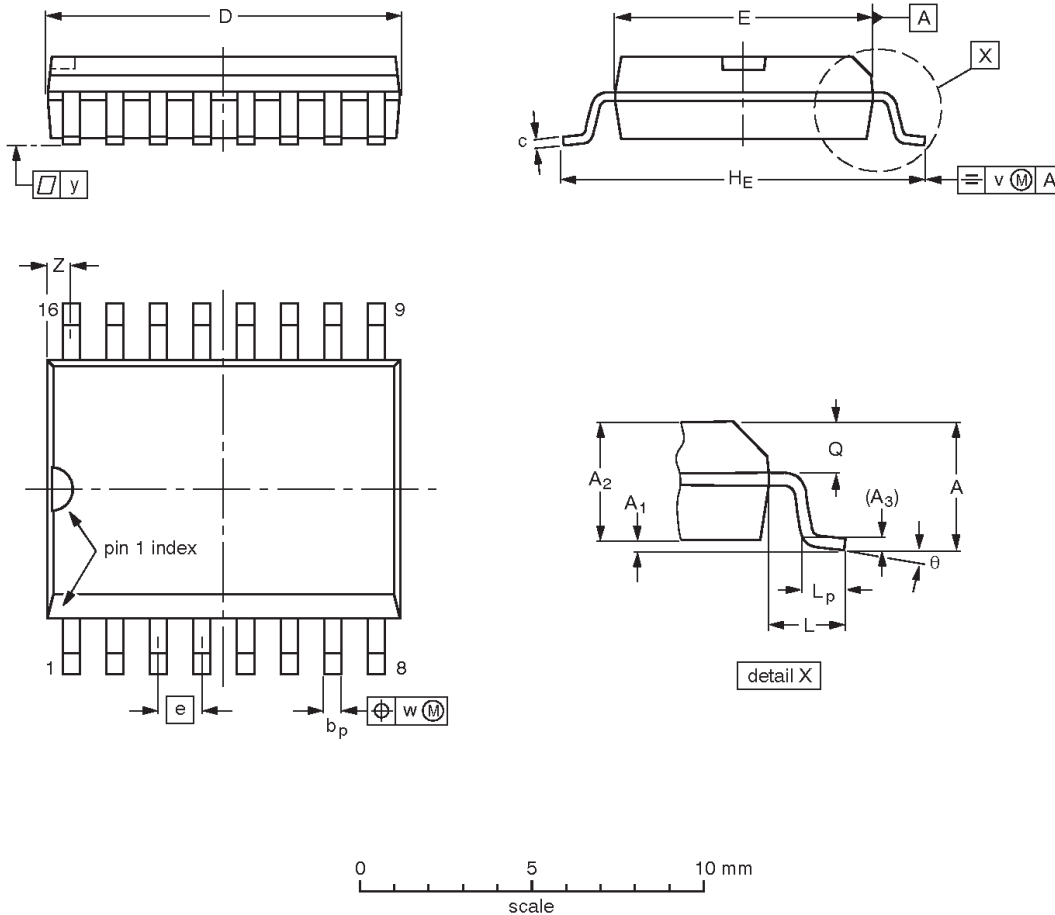
- $C_b$  = total capacitance of one bus line in pF.
- $t_{VD,ACK}$  = time for Acknowledgement signal from SCL low to SDA (out) low.
- $t_{VD,DAT}$  = minimum time for SDA data out to be valid following SCL low.

8-bit I<sup>2</sup>C and SMBus I/O port with interrupt

PCA9554/PCA9554A

SO16: plastic small outline package; 16 leads; body width 7.5 mm

SOT162-1



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	10.5 10.1	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.41 0.40	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

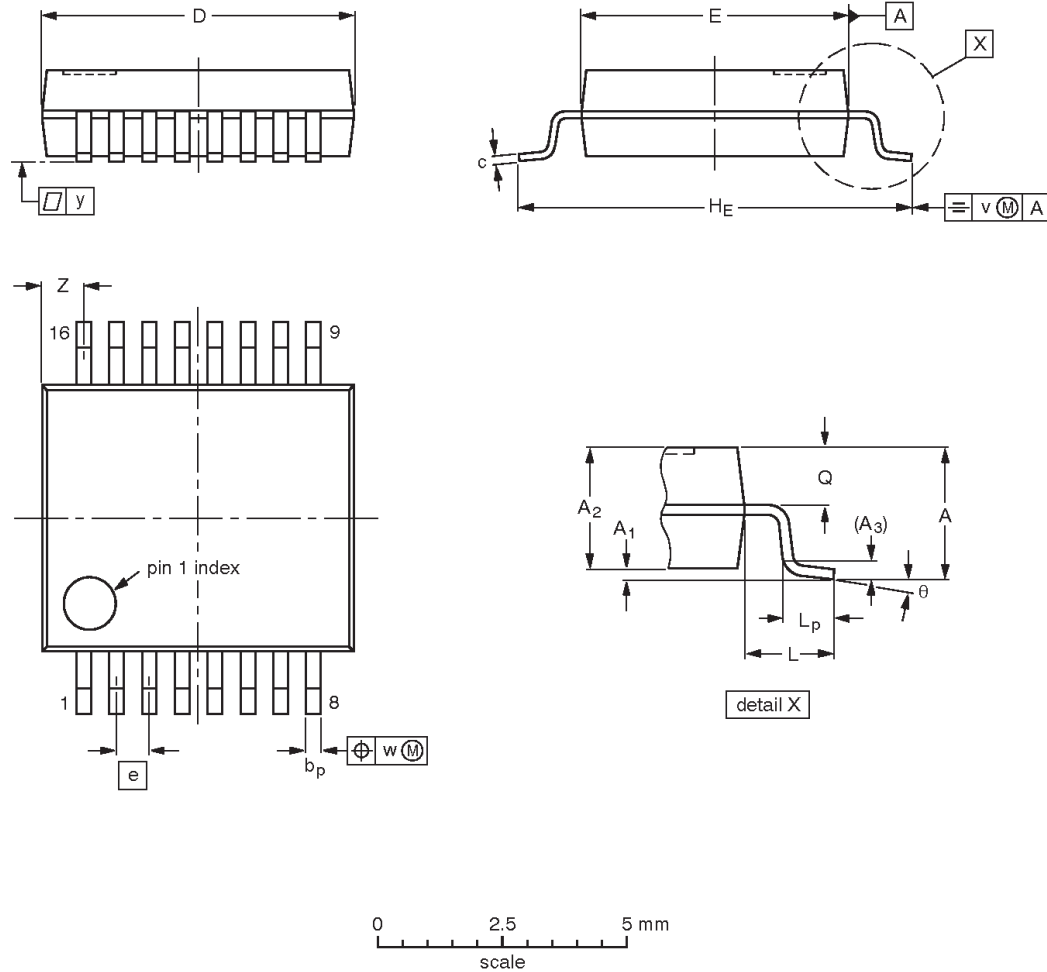
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT162-1	075E03	MS-013				-97-05-22 99-12-27

8-bit I<sup>2</sup>C and SMBus I/O port with interrupt

PCA9554/PCA9554A

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	$\theta$
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8° 0°

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

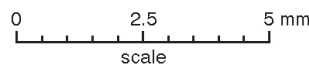
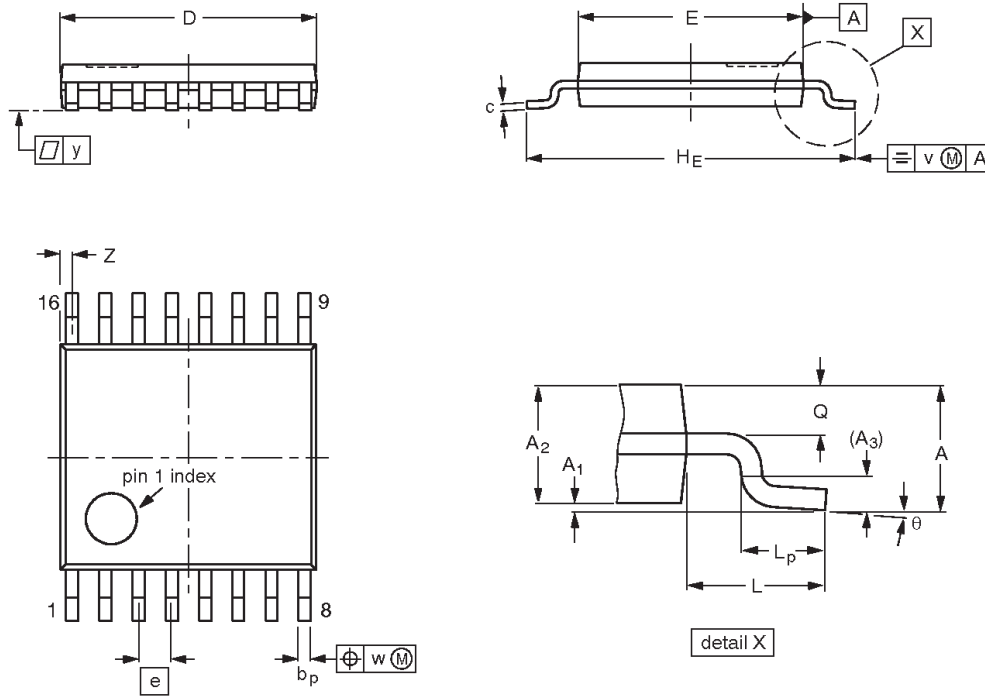
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
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SOT338-1		MO-150				95-02-04 99-12-27

8-bit I<sup>2</sup>C and SMBus I/O port with interrupt

PCA9554/PCA9554A

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

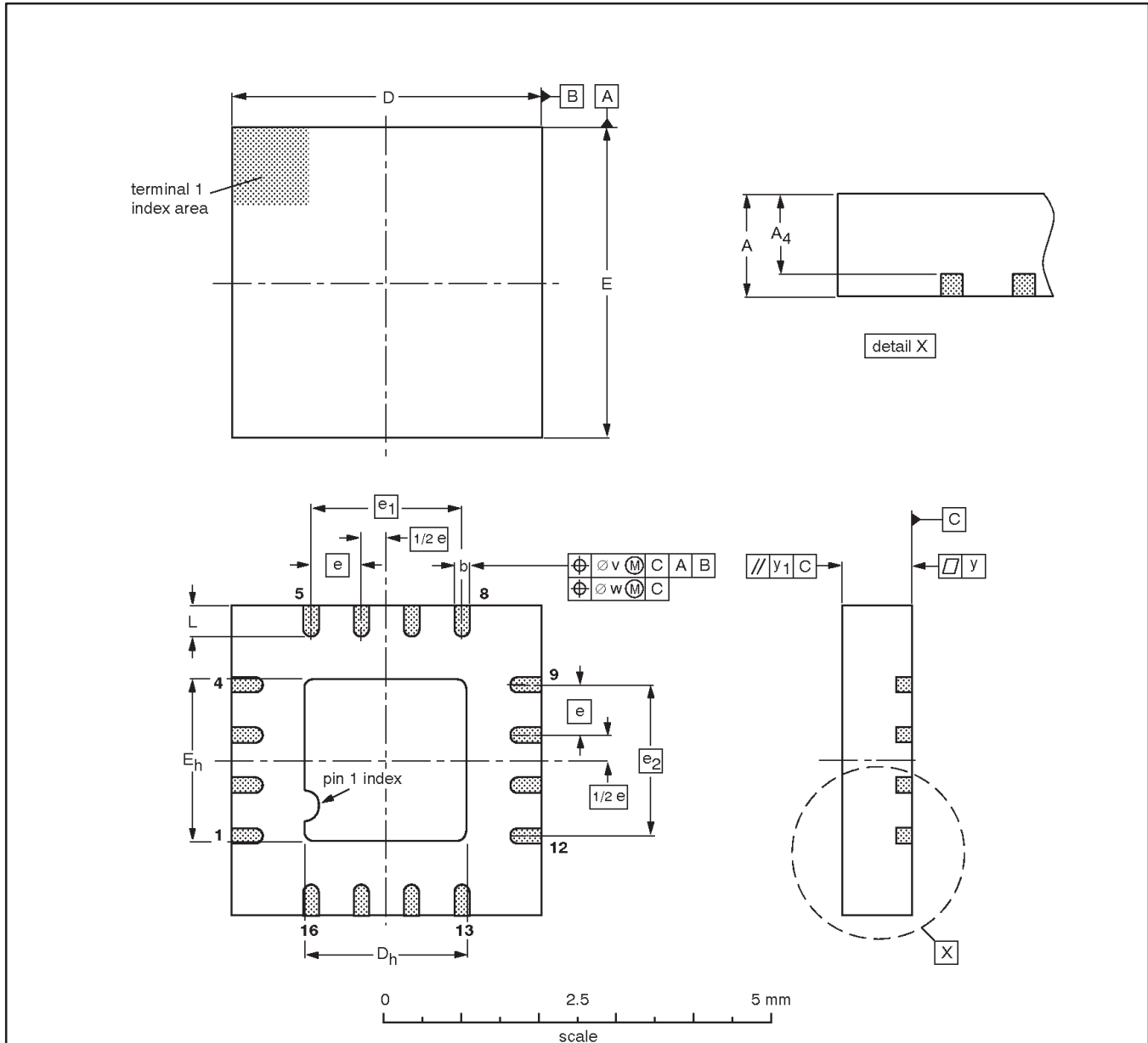
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT403-1		MO-153				95-04-04 99-12-27

# 8-bit I<sup>2</sup>C and SMBus I/O port with interrupt

# PCA9554/PCA9554A

**HVQFN16:** plastic heatsink very thin quad flat package; no leads; 16 terminals; body 4 x 4 x 0.85 mm

**SOT629-1**



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>4</sub> max.	b	D <sup>(1)</sup>	D <sub>h</sub>	E <sup>(1)</sup>	E <sub>h</sub>	e	e <sub>1</sub>	e <sub>2</sub>	L	v	w	y	y <sub>1</sub>
mm	1.00	0.80	0.40 0.23	4.05 3.95	2.25 1.95	4.05 3.95	2.25 1.95	0.65	1.95	1.95	0.75 0.50	0.2	0.1	0.05	0.1

**Note**

1. Plastic or metal protrusions of 0.076 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT629-1		MO-220				<del>01-06-20</del> 01-08-08

8-bit I<sup>2</sup>C and SMBus I/O port with interrupt

PCA9554/PCA9554A



Purchase of Philips I<sup>2</sup>C components conveys a license under the Philips' I<sup>2</sup>C patent to use the components in the I<sup>2</sup>C system provided the system conforms to the I<sup>2</sup>C specifications defined by Philips. This specification can be ordered using the code 9398 393 40011.

## Data sheet status

Data sheet status <sup>[1]</sup>	Product status <sup>[2]</sup>	Definitions
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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## Contact information

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